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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,280	01/10/2002	Mark Elliott Hack	AUS920011014US1	4451

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EXAMINER	
LOHN, JOSHUA A	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 09/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/045,280	HACK ET AL.
	Examiner	Art Unit
	Joshua A Lohn	2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claim 26 recites the limitation "said exception handler routine" in line 29 of page 25. There is insufficient antecedent basis for this limitation in the claim. For the purpose of examination the claim will be interpreted to read similarly to claims 13 and 39 where instead of "said exception handler routine for requesting said service processor to deconfigure", as stated in claim 26, it will be interpreted to read "requesting, utilizing said error handler routine, said service processor to deconfigure", as recited in claims 13 and 39, which seems to be the intended meaning.

Claim Rejections - 35 USC § 103

Claims 1-3, 6-9, 13-16, 19-22, 26-29, 32-35, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arndt, United States Patent number 6,658,591, filed June 8, 2000, in view of Bossen et al., United States Patent number 6,516,429, filed November 4, 1999.

As per claim 1, Arndt discloses a method for preventing machine crashes due to hard errors in one of a plurality of processors in a logically partitioned data processing system (Arndt, col. 6, lines 6-24), said method comprising the steps of: detecting an error in one of said plurality of processors (Arndt, col. 8, lines 49-67); determining when the processing of the error is complete and rebooting the configured ones of the plurality of processors only in response to a determination that the one of the plurality of processors has been dealt with (Arndt, col. 9, lines 1-7, where the system is rebooted after the error information has been entered in the log to deal with the problems). Arndt fails to disclose the use of deconfiguration in the handling of the error before resetting the system.

Bossen discloses deconfiguring the system in response to a failure to prohibit the use of the use of the system in the event of a restart (Bossen, col. 4, lines 55-67).

It would have been obvious to one skilled in the art at the time of the invention to use the deconfiguration of Bossen in the invention of Arndt.

This would have been obvious because both Arndt and Bossen keep a record of a failure of a processor (Arndt, col. 9, lines 1-2, with a log record, and Bossen, col. 4, lines 65-67). Arndt further discloses a desire to reboot the system and continue operation without the failed processor (Arndt, col. 9, lines 1-7). Bossen discloses a method to allow for the reboot and continuation without starting the failed processor through the use of the stored failure record, which exists in both inventions as mentioned above (Bossen, col. 7, lines 5-15). It would have been obvious to use this additional aspect of the fault logging provided by Bossen to allow for the invention of Arndt to fully ignore the failed processor, as desired in a disclosed embodiment (Arndt, col. 9, lines 1-7).

As per claim 2, the combined invention of Arndt and Bossen discloses the step of in response to said detecting an error, requesting deconfiguration of said one of said plurality of processors (Bossen, col. 4, lines 12-43).

As per claim 3, the combined invention of Arndt and Bossen discloses the step of in response to said one of said plurality of processors being deconfigured, providing an indication that said one of said plurality of processors has been deconfigured (Bossen, col. 4, liens 55-67, and Arndt, col. 9, lines 1-7).

As per claim 6, the combined invention of Arndt and Bossen discloses the steps of: receiving a request to deconfigure said one of said plurality of processors (Bossen, col. 4, lines 12-43); deconfiguring said one of said plurality of processors (Bossen, col. 4, lines 55-67); and storing an indication of deconfiguration in response to a completion of deconfiguring said one of said plurality of processors (Bossen, col. 4, lines 55-67, and Arndt, col. 9, lines 1-7).

As per claim 7, the combined invention of Arndt and Bossen discloses the step of storing said indication in non-volatile memory (Bossen, col. 4, lines 64-67).

As per claim 8, the combined invention of Arndt and Bossen discloses the steps of: providing a service processor within said logically partitioned data processing system; in response to said detecting an error (Bossen, col. 4, lines 12-26), deconfiguring said one of said plurality of processors utilizing said service processor (Bossen, col. 4, lines 55-67); and providing, utilizing said service processor, an indication that said one of said plurality of processors has been deconfigured (Bossen, col. 2, line 65 through col. 3, line 1).

As per claim 9, the combined invention of Bossen and Arndt disclose the detecting of an error in one of the plurality of processors where the error is a hard error (Bossen, col. 4, lines 22, where the pattern leads to a hard error detection).

As per claim 13, Arndt discloses a method for preventing machine crashes due to hard errors in one of a plurality of processors in a logically partitioned data processing system (Arndt, col. 6, line 6-24) providing an error handler routine and detecting, utilizing said error handler routine, an error in one of said plurality of processors (Arndt, col. 8, lines 49-67); in response to said error handler routine detecting an error and determining that an indication has been stored

indicating that the error is dealt with; requesting, utilizing said error handler routine, a reboot of configured ones of said plurality of processors; and rebooting, utilizing said service processor, said configured ones of said plurality of processors (Arndt, col. 9, lines 1-7, where the system is rebooted after the error information has been entered in the log, which indicates the completion of the processing of the error). Arndt fails to disclose the use of a service processor and deconfiguration in the handling of the error and only completing the deconfiguration finishing the reboot process mentioned above.

Bossen discloses providing a service processor within said logically partitioned data processing system and requesting, utilizing an error handler routine, said service processor to deconfigure said one of said plurality of processors (Bossen, col. 4, lines 12-43); deconfiguring, utilizing said service processor, said one of said plurality of processors (Bossen, col. 4, lines 55-67); in response to a completion of said deconfiguration of said one of said plurality of processors, storing, utilizing said service processor, an indication in a non-volatile memory that said one of said plurality of processors has been deconfigured (Bossen, col. 4, lines 55-67).

It would have been obvious to one skilled in the art at the time of the invention to use the deconfiguration of Bossen in the invention of Arndt.

This would have been obvious because both Arndt and Bossen keep a record of a failure of a processor (Arndt, col. 9, lines 1-2, with a log record, and Bossen, col. 4, lines 65-67). Arndt further discloses a desire to reboot the system and continue operation without the failed processor (Arndt, col. 9, lines 1-7). Bossen discloses a method to allow for the reboot and continuation without starting the failed processor, through the use of the stored failure record, which exists in both inventions as mentioned above (Bossen, col. 7, lines 5-15). It would have

been obvious to use this additional aspect of the fault logging provided by Bossen to allow for the invention of Arndt to fully ignore the failed processor, as desired in a disclosed embodiment (Arndt, col. 9, lines 1-7).

As per claims 14-16, 19-22, and 26, these claims are merely a system for implementing the methods of claims 1-3, 6-9, and 13 respectively, and as such are rejected under the same grounds mentioned above.

As per claims 27-29, 32-35, and 39, these claims are merely a system for implementing the methods of claims 1-3, 6-9, and 13 respectively, and as such are rejected under the same grounds mentioned above.

Claims 4, 5, 17, 18, 30, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arndt '591 in view of Bossen '492, in further view of Microsoft Computer Dictionary, Fourth Edition, published by Microsoft Pres in 1999.

As per claim 4, the combined invention of Arndt and Bossen discloses the steps of: detecting said error in said one of said plurality of processors (Arndt, col. 8, lines 49-67); determining whether said one of said plurality of processors has been deconfigured (Arndt, col. 7, lines 1-7, and Bossen, col. 4, lines 55-67, where the combined error logging indicates the deconfiguration); and requesting a reboot of said configured ones of said plurality of processors (Arndt, col. 7, lines 1-7). Arndt and Bossen fail to disclose these steps being executed by an exception handler.

Microsoft Computer Dictionary discloses that exception handling is a situation in which a separate routine must be used to deal with a problem in the conditions of the system (Microsoft Computer Dictionary, page 173).

It would have been obvious to one skilled in the art at the time of the invention to interpret the service processor utilized in the combined invention of Arndt and Bossen to function as an exception handler (Bossen, col. 4, lines 55-67).

This would have been obvious because Bossen discloses using the service processor to halt the system execution of the offending processor in order to service the error (Bossen, col. 4, lines 55-67). This obviously shows the use of an external routine to deal with the problem generated by the errors and would result in the service processor system of Arndt and Bossen functioning equivalently to an exception handler, as defined above.

As per claim 5, the combined invention of Bossen and Arndt, in view of the Microsoft Computer Dictionary discloses the step of requesting, utilizing said exception handler routine, said one of said processors be deconfigured (Bossen, col. 4, lines 12-43).

As per claims 17 and 18, these claims are merely a system for implementing the methods of claims 4 and 5 respectively, and as such are rejected under the same grounds mentioned above.

As per claims 30 and 31, these claims are merely a system for implementing the methods of claims 4 and 5 respectively, and as such are rejected under the same grounds mentioned above.

Claims 10-12, 23-25, and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arndt '591 in view of Bossen '492, in further view of Arndt '932, United States Patent Application Publication number US 2003/0023932, filed March 29, 2001.

As per claim 10, the combined invention of Bossen and Arndt '591 disclose the detecting of an error in one of the plurality of processors. Bossen and Arndt '591 fail to disclose the explicit detection of an address translation error.

Arndt '932 discloses the detection of address translation errors in processors that can generate a system crash (Arndt '923, ¶23).

It would have been obvious to include the address translation error in the definition of the errors detected by the system of Bossen and Arndt '591.

This would have been obvious because the combined invention of Bossen and Arndt '591 discloses a desire to detect errors within a processor (Bossen, col. 4, lines 12-27). Arndt '923 merely points out one of the many types of errors that may be detected in a system. It would have been obvious to include the error detected in Arndt '923 in the invention of Bossen and Arndt '591 to gain the benefit of detecting a greater variety of errors in the processor.

As per claim 11, the combined invention of Bossen and Arndt '591 disclose the detecting of an error in one of the plurality of processors. Bossen and Arndt '591 fail to disclose the explicit detection of a translation look aside buffer address translation error.

Arndt '932 discloses the detection of translation look aside buffer address translation errors in processors that can generate a system crash (Arndt '923, ¶23).

It would have been obvious to include the translation look aside buffer address translation error in the definition of the errors detected by the system of Bossen and Arndt '591.

This would have been obvious because the combined invention of Bossen and Arndt '591 discloses a desire to detect errors within a processor (Bossen, col. 4, lines 12-27). Arndt '923 merely points out one of the many types of errors that may be detected in a system. It would have been obvious to include the error detected in Arndt '923 in the invention of Bossen and Arndt '591 to gain the benefit of detecting a greater variety of errors in the processor.

As per claim 12, the combined invention of Bossen and Arndt '591 disclose the detecting of an error in one of the plurality of processors. Bossen and Arndt '591 fail to disclose the explicit detection of a data effective to real address translation error.

Arndt '932 discloses the detection of data effective to real address translation errors in processors that can generate a system crash (Arndt '923, ¶23).

It would have been obvious to include the data effective to real address translation error in the definition of the errors detected by the system of Bossen and Arndt '591.

This would have been obvious because the combined invention of Bossen and Arndt '591 discloses a desire to detect errors within a processor (Bossen, col. 4, lines 12-27). Arndt '923 merely points out one of the many types of errors that may be detected in a system. It would have been obvious to include the error detected in Arndt '923 in the invention of Bossen and Arndt '591 to gain the benefit of detecting a greater variety of errors in the processor.

As per claims 23-25, these claims are merely a system for implementing the methods of claims 10-12 respectively, and as such are rejected under the same grounds mentioned above.

As per claims 36-38, these claims are merely a system for implementing the methods of claims 10-12 respectively, and as such are rejected under the same grounds mentioned above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure is provided on form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua A Lohn whose telephone number is (703) 305-3188. The examiner can normally be reached on M-F 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoleil can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SCOTT BADERMAN
PRIMARY EXAMINER